

IBM Docket No.: POU920010050 Ser. No. 09/841569:

Examiner: Mujtaba M Chaudry



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE  
BOARD OF PATENT APPEALS AND INTERFERENCES

Assistant Commissioner for Patents

Washington, D.C. 20231

Attn: BOARD OF PATENT APPEALS AND INTERFERENCES

In re: Patent Appln. USSN: 09/841,569 Filed: April 24, 2001 Action Day: 9/16/05

Title: Method and apparatus for ABIST Diagnosis.

Inventor(s): J. E. Eckleman et al

Examiner: Mujtaba M. Chaudry

Group 2133

Attorney Docket No. POU920010050US1

Attorney/Agent Lynn L. Augspurger, Reg. No. 24,227. Deposit Acct. 09-0463

APPEAL BRIEF ON APPEAL FROM THE EXAMINER TO THE BOARD OF  
PATENT APPEALS AND INTERFERENCES

Sir:

This appeal is taken under 37 CFR 1.191 by the applicants for a patent with respect to all claims which have been twice rejected, and who have been given a final rejection in the action of the Examiner dated September 16, 2005.

This brief is filed in triplicate together with the requisite fees authorized by the accompanying fee authorization to be charged to Deposit Account No. 09-0463.

This Brief has the following Contents:

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### BRIEF ON APPEAL

1) REAL PARTY IN INTEREST: The real party in interest is the Assignee of all interest as recorded 4/24/2001 Reel/Fram: 011766/0403, namely: International Business Machines Corporation, New Orchard Road, Armonk, New York 10504.

(2) RELATED APPEALS AND INTERFERENCES: None.

(3) STATUS OF CLAIMS: All claims (1-7) in the application stand rejected. Each of claims 1 through 7 are on appeal.

(4) STATUS OF AMENDMENTS: No amendment has been filed after the final rejection. Claim 1 was amended on July 29, 2005. No other claims have been amended upon filing of the RCE; however, claims 2, 3,4,5 and 7 were previously amended. The claims on appeal are in the Appendix of Claims.

(5) SUMMARY OF INVENTION: Generally, the application has been directed to seven claimed inventions each of which a method for real time capture of desired firing chip cell diagnostic information for high speed testing of a semiconductor chip by assembly test after scan initialization of LSSD diagnostic registers on the semiconductor chip, said level of assembly test being selected from any level of a group consisting of: an initial manufacturing wafer test, a module test, a system level test, regardless of the clocking methodology. relate to a digital temperature sensor for monitoring temperature in a memory subsystem.

DTS-T2(70) and DAC-FAN (80) as described on page 8 of the application and shown in Figure 1.

. For a concise explanation of the invention defined in the claims involve in appeal, refer to the specification and drawings identified in the claims which follow.

(6) ISSUES: With respect to all claims, the primary issue on appeal is whether each claim 1-7) is unpatentable under 35 U.S.C. 103(a) over Yasui (USPN 6594788B1) further in view of Sato (USPN 5790559) for the same reasons repeated in the Final Office Action dated September 16, 2005.

(7) GROUPING OF CLAIMS: Each claim differs in claimed subject matter, and for the purposes of this appeal the claimed grouping of claims does not stand or fall together. All claims require that the method claimed is "for high speed testing of a semiconductor chip by assembly

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test after scan initialization of LSSD diagnostic registers on the semiconductor chip, said level of assembly test being selected from any level of a group consisting of: an initial manufacturing wafer test, a module test, a system level test, regardless of the clocking methodology. relate to a digital temperature sensor for monitoring temperature in a memory subsystem" as required by Claim 1. The reasons for this are illustrated in the previous summary of the invention and in the argument which follows. For convenience of understanding, all claims are dependent upon claim 1, and each claim 2-6 further is dependent upon the next higher numbered claim, while claim 7 is dependent upon claim 1..

#### (8) ARGUMENT:

Remember, under 35 USC 103 it is "the invention as a whole that must be considered in obviousness determinations. The invention as a whole embraces the structure, its properties, and the problem it solves.... whether what the inventor did would have been obvious to one of ordinary skill in the art attempting have been obvious to one of ordinary skill in the art attempting to solve the problem upon which the inventor was working." *Wright, in re: 6 USPQ2d 1959, 1961, CA FC 1988*. Respectfully, this rejection does not conform to the requirements of MPEP 706.02, which requires not only that prior art rejections should be strictly confined to the best available art (certainly that art cited by the applicant is better than that art used) as the primary reference, but also, in a PTO action with respect to each claim, in addition, if there are differences a rejection based on 35 USC 103, ".... there should be set forth (1) the difference or differences in the claim over the applied reference(s), (2) the proposed modification of the applied reference(s) necessary to arrive at the claimed subject matter, and (3) an explanation why such proposed modification would be obvious." (MPEP Sec. 706.02).

Judge Rich, see *Ryco In. v. Av-Bar Corp.* 705 8 USPQ2d 1325 for the Federal Circuit Court of Appeals, stated that one question which must be answered in the affirmative to support a case of obviousness under 35 USC 103 is: "Do the elements of the reference perform the same function as those of the claim in issue?" This is not whether the elements or steps of a reference are similar in name only and not in function. To perform a computer search to find common words is not such an investigation. It is not enough if the prior art reference elements of the same name are found in a reference, if they generally perform a different function not directed to the claimed invention.. This is particularly true when the claimed arrangement is contrary to the teaching of the principal (here only on principal patent is cited) prior art patent. Thus critical differences, which include different functions, teachings away, and other criteria need to be recognized by the Patent Office as facts which will not support a conclusion of obviousness, rather than be passed off obvious as has been done in this last action.. These critical differences are one of the four factual inquiries under *Graham* pertinent to any obviousness query. Furthermore, obviousness cannot be established by combining the teaching of the prior art to produce the claimed invention, absent some teaching, suggestion or incentive to supporting the combination. See: *In re Bond* 15 USPQ2d 1566, 1568 (FCCA 1990). While it may not be necessary that a cited reference or prior art specifically suggest making a combination, it is necessary that there must be some teaching, reason, suggestion, or motivation to produced the claimed device.

Did Yuasi US Patent 6594788 teach one of ordinary skill in the art attempting to solve the problem upon which the inventors were working to provide those things needed "for high speed

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testing of a semiconductor chip by assembly test after scan initialization of LSSD diagnostic registers on the semiconductor chip, said level of assembly test being selected from any level of a group consisting of: an initial manufacturing wafer test, a module test, a system level test, regardless of the clocking methodology. relate to a digital temperature sensor for monitoring temperature in a memory subsystem" as required by claim 1? We think the answer must be NO.

Yuasi US Patent 6594788 relates to a memory testing apparatus for testing semiconductor memories with a external memory testing apparatus separate from the memory under test, column 2, line 23. Indeed as the background of the invention explained external memory testing apparatus has many problems, including not being able to apply a test algorithm at a failing cycle time; are insufficient to detect failures which rely on on-chip clock frequency multiplication techniques to multiple tester provided clock signal frequencies; are insufficient for line monitoring activity or identification of nonrandom manufacturing defects (mask defects known as "repeaters) in interactive procedures (background of the invention page 3).

While tacitly admitting that the claim language does not teach how to implement on chip testing when, as claimed "said level of assembly test being selected from any level of a group consisting of: an initial manufacturing wafer test, a module test, a system level test, regardless of the clocking methodology", this limitation has been dismissed by stating that "Surely the reference teach at least one if not all of the possible level" and "Furthermore, these various levels of tests are well known in the art and cannot render the claims patentably distinct or non-obvious, and "Similar reason applies for on chip testing", citing In re Larson, Russler and Meldahl, 144 USPQ 347 for some reason which is not apparent from the reading of that 1965 decision relating to an "integral" disc brake and clamp. Such backhanded application of MPEP 2144.03 is not judicious, and it is unwarranted. The best art the examination applied, if Yuasi USPATENT 6594788 only tested individual memory chips (see Fig. 5, 119 MUT) something which is not any of the selected "an initial manufacturing wafer test, a module test, a system level test, regardless of the clocking methodology" of the claim.

Furthermore, the principal reference US Patent 6594788 is not one which performs assembly test after scan initialization of LSSD diagnostic registers on a semiconductor chip. There are no LSSD diagnostic registers on the 119 MUT of Yuasi US Patent 6594788.

As there are no LSSD diagnostic registers of the semiconductor chip being tested, the initial requirement of the claim of "collecting data from scanning the circuits of said semiconductor chip having LSSD diagnostic registers on chip for a failing cell for desired handling of multiple failures on a failing chip for immediate scan-out off-chip at a level of assembly test after scan initialization of the LSSD diagnostic registers on the semiconductor chip" is not shown, taught or suggested by US Patent 6594788.

Furthermore, as the claim requires that the level of assembly test after scan initialization of the LSSD diagnostic registers be selected, and the claim states "said level of assembly test being selected from any level of a group consisting of: an initial manufacturing wafer test, a module test, a system level test, regardless of the clocking methodology"

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**So there is not even the basic first element of the claimed subject matter present in the US Patent**

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So it is clear that the elements of King do not perform the same function as those of the claim 1 in issue

The basic premise of the examination would not convince one skilled in the art to combine the references to achieve

The examination did not even address the missing elements in the combined references in the final rejection.

Thus the function of the claim is not met even by the combination of the references alluded to by the examination, even in the most general sense, and certainly not in the specific sense of the claimed elements and their interrelationship and function on a chip for testing at any level in the manufacturing process with the same elements.

When the applicants filed an RCE they added further limitations in the claim, but received only a repetitious response, not a new examination. The applicants said:

The applicants point out that the examiner has already found the limitation of N+1 in claim 1 was not in the art and that process is elaborated with this amendment. The references only show apparatus incapable of handling multiple failures on a chip diagnosis of fault, and do not show any on chip apparatus or process for handling multiple bit failure detection. They do not show the skipping process for reuse of chip circuitry, as the examiner has noted. The specific step by step method claimed is not shown by the references. To say that there is a programmable tester which can be created by a user and loaded in advance does not teach the invention. Those skilled in the art would recognize that the references cited by the examiner are external to the chip being tested and not on chip as in the claimed invention, and there is no teaching in any reference cited how to implement on chip testing at any level specified in the claims.

Both references cited by the examiner relate to external testers. In the case of Yasui 6594788 the device being tested is a memory under test 119.

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Claim 1 specifies that the semiconductor circuit being tested is one *"having LSSD diagnostic registers on chip for a failing cell for desired handing of multiple failures on a failing chip for immediate scan-out off-chip at a level of assembly test after scan initialization of the LSSD diagnostic registers ~~of~~ on the semiconductor chip"*. The memory under test 119 of Yasui does not meet this limitation.

Claim 1 further specifies that the test occurs in *"said level of assembly test being selected from any level of a group consisting of: an initial manufacturing wafer test, a module test, a system level test, regardless of the clocking methodology"*, something that can't occur in the memory under test 119 of Yasui.

In fact, the memory under test 119 of Yasui does not have any way of for providing: ***the desired failing chip handling on chip of multiple bit failure detection*** by any means at all.

Furthermore the claim 1 specifies that the on chip multiple bit failure detection occurs by:

*providing data collection of a first failing cell in said LSSD diagnostic registers, and then skipping the collection of data up to a programmed amount to skip up to a subsequent failing cell.*

Neither Yasui which tests MUT 119 nor Sato 5790559 which tests ECL semiconductor memory 206 provide this kind of data collection in LSSD diagnostic registers located on chip (indeed the elements tested by Masui and Sato are different, and there is no apparent similarity gving rise to a desireability of combining elements of the two external testers and what would be the effect of a combination). There is no skipping data collection a programmed

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amount to skip up to a subsequent failing cell and no reuse of on chip logic. Neither Yasui nor Sato even talk about skipping up to a subsequent failing cell with their external testers. They can't test a semiconductor chip at any of the levels required by the claim, i.e. at any of the test levels of: an initial manufacturing wafer test, a module test, a system level test.

Indeed, they don't provide further as specified in the claim 1, for:

*recording the failure of a next failing cell recognized after said subsequent failing cell in said LSSD diagnostic registers while making reuse of logic including existing address registers for providing data synchronous with fail determination circuits for data collection used for collection of data of said first failing cell, and then*

*pinpointing an actual failure for said next failing cell using additional data collected by reuse of the logic for data collection used for collection of data of said first failing cell.*

The applicants' contend that further, none of the steps set out in the dependent claims are shown in the art relied upon by the examiner. The applicants contend that each of the dependent claims is independently patentable, they not only incorporate each step of the independent claim which is not shown in the art, but also additional features which are not shown in the art.

As stated in a Judge Rich decision, see *Ryco In. v. Av-Bar Corp.* 705 8 USPQ2d 1325 the Federal Circuit Court of Appeals stated that one question which must be answered in the affirmative to support a case of obviousness under 35 USC 103 is: "Do the elements of the reference perform the same function as those of



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the claim in issue?" Here the applicants contend that there is in the reference no on chip failure detection which applies to more than one failure identification, after detection of a first failure, which can be found at **any of the test levels of: an initial manufacturing wafer test, a module test, a system level test.**

The applicants would repeat these statements here on appeal, as the examination still has no argument which supports an conclusion of obviousness.

If one were to review again the invention as a whole as stated in claim 1, directed to " the solution expressed in Claim 1, and each of the separate inventions expressed in the dependent claims, embraces a different structure (everything is on chip and in hardware employing LSSD diagnostic registers not found in any reference), different properties (**the desired failing chip handling on chip of multiple bit failure detection**), and different problems (on chip failure detection which applies to more than one failure identification, after detection of a first failure, and at **any of the test levels of: an initial manufacturing wafer test, a module test, a system level test**) (than solved by the references used in hindsight to allege "obviousness").

The unanswered differences, which include different functions, teachings away, and other criteria need to be recognized by the Patent Office as facts which will not support a conclusion of obviousness. These critical differences are one of the four factual inquiries under Graham pertinent to any obviousness query. Furthermore, obviousness cannot be established by combining the teaching of the prior art to produce the claimed invention, absent some teaching, suggestion or incentive to supporting the combination, and here none is stated in the Art itself, but only in the argument of the Examination. It is the art's teaching that must be examined..

The applicants believes that each additional claimed elements in the dependant claim add patentable subject matter, and the examination has not addressed each additional claim, as required. Indeed, the use of an external microcontroller is not used and not needed in the invention of this application, and yet the Examination requires this to be used as a matter of obviousness.

Unanswered is the claim, as expressed in claim 2 that there is invention in a combination of Claim 1 with Claim 2, adding to claim 1, was also rejected by the Examination by something completely unrelated to determination of **the desired failing chip handling on chip of multiple bit failure detection**, with on chip failure detection which applies to more than one failure identification,

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after detection of a first failure, and at any of the test levels of: an initial manufacturing wafer test, a module test, a system level test, which also has "on chip with supplemental address registers which supplement said existing address registers for providing data synchronous with fail determination circuits, employing ABIST comparison circuit to obtain a bit wise fail result vector corresponding to each device data out of a device under test, and wherein said bit wise fail result vector feeds a detect and encode circuit that determines if one and only one device data out failed, and if so, provides an encoded "address" that is concatenated to a corresponding register address field." The LLSD diagnostic registers use ABIST comparison circuits as described, and neither the LSSD diagnostic registers, the additional supplemental address registers, or the ABSIST comparison circuit as described is shown in the combined references, let alone one chip which has all claimed elements and functions.

As to the final rejection of the claim 3, as expressed in claim 3 there is again no on chip circuit for performing testing using LSSD diagnostic registers. Instead the rejection says that all things can be obtained with an external memory controller programmed in some way or another not applicable to the hardware claimed. The rejection is not relevant to the invention in a combination of Claim 1 with Claim 2, and adding with claim 3 "wherein said bit wise fail result vector is fed thereafter into a hold and compare function circuit having a hold portion of the function providing for the "full" fail address field comprising multiple bits of the memory address of the device under test plus the failing output encoded address for identifying the failing location to be stored in a LSSD register of said semiconductor chip, and wherein the compare function provides for identification recording of subsequent unique and different failing locations to be identified in the device under test." The references do not have the ABIST comparison circuit to obtain a bit wide fail result vector corresponding to each device data out of a device under test, and therefore can't support or teach the hold and compare function circuit, which is not provided in the reference, for providing identifying bits to be stored in an LSSD register which is also not present, where the compare function provides for identification recording of subsequent unique and different failing locations to be identified in the device under test.

Apparently realizing that the principal reference is not applicable, the examination in rejecting claims 4-7 relies on Sato which is an external testing controller for testing a memory under test mounted in a testing apparatus, not one which can test at any of the test levels of: an initial manufacturing wafer test, a module test, a system level test. Unanswered is the specific language of the claims.

Unanswered is the claim, as expressed in claim 4 that there is invention in a combination of Claim 1 with Claim 2, with Claim 3 and adding with claim 4 "wherein said hold and compare function circuit is configured to load the first and reload each subsequent unique failing location encountered,

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decrementing a programmable skip counter at each unique fail encountered, until said programmable skip counter reaches a final "zero" state." The circuit is not supported in the references.

Unanswered is the claim, as expressed in claim 5 that there is invention in a combination of Claim 1 with Claim 2, with Claim 3 and adding with claim 4, the limitations of claim 5 reading:

5. (Previously Amended) The method according to claim 4 wherein said hold and compare function circuit is configured to load the first and reload each subsequent unique failing location encountered, decrementing a programmable skip counter at each unique fail encountered, until the skip counter reaches an intended next failing cell recognized fail to be recorded." The examination admits that there is not in the references any teaching of the programmable skip counter on the chip under test, so how can also not present in the references compare function circuit load the first and reload each subsequent unique failing location encountered, and decrement a programmable skip counter at each unique fail encountered until the skip counter reaches an intended next failing cell recognized fail to be recorded. This rejection cannot be supported.

Unanswered is the claim 6, as expressed in a claim 6 that there is invention in a combination of Claim 1 with Claim 2, with Claim 3, with claim 4, with claim 5, and adding with claim 6, the limitations of claim 6, reading:

6. (Original) The method according to claim 5 wherein said hold and compare function circuit allows said programmable skip counter to record a zero state as a default thus enabling the first fail to be recorded." There is no compare function circuit that allows a programmable skip counter to record a zero default state in Sato.

And also unanswered is the specific language of claim 7, as expressed in claim 7 that there is invention in a combination of Claim 1 with Claim 2, with Claim 3, with claim 4, with claim 5, and adding in combination with claim 6, the limitations of claim 7 reading:

The method according to claim 2 wherein said supplemental address registers which supplement said existing address registers for providing data synchronous with fail determination circuits include a fail trap register, and there is provided a programmable skip counter, and a hold and compare function circuit, and wherein said programmable skip counter is enabled for initialization to a "record first fail" mode, and then with non-zero values of the programmable skip counter to a "record a next fail" mode, wherein said "record first fail" mode is

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considered the default or base function when the initial state of all registers is defined to be "0", and is obtained through scan initialization of the LSSD registers of the semiconductor chip

There is not teaching in Sato about this. It is noted in the RCE that the dependency on claim 2 was mistyped. That matter is corrected in the appendix of claims.

The applicants are unable to find any teaching of the claim matter of the primary or dependent claims in the references relied upon by the examiner. It does not readily come to mind how even with hindsight of the application that anyone skilled in the art can combine specific teaching of the references to meet the claims submitted, nor even what the Examination alleges is there, which is not in any event what is the claimed matter. No one to one comparison of a combination is possible or discussed in the examination.

The invention was after the applicants' employer could not find a commercial solution to the needs of the applicants' assignee. Certainly the argument waiving a external controllers and test units around without even understanding the claims made to a need to have on chip a test that could be applied at any of the test levels of: an initial manufacturing wafer test, a module test, a system level test is not taught or suggested by any reference.

As supported by the detailed description and drawings the art does not have such as to meet the requirements for a rejection of claims under 35 USC 103. Does not the PTO rule continue to be that a requires not only that prior art rejections should be strictly confined to the best available art (Yausi US Patent 6594788 is the primary reference and understood to be the best available art), but also, in a PTO action with respect to each claim, in addition, if there are differences a rejection based on 35 USC 103, "... there should be set forth (1) the difference or differences in the claim over the applied reference(s), (2) the proposed modification of the applied reference(s) necessary to arrive at the claimed subject matter, and (3) an explanation why such proposed modification would be obvious." This examination lacks these necessities.

Further, it should be remembered that the applicants claim all claims are independently patentable, as it has been demonstrated that no claim is shown in the art. The applicants do argue that the claims are separately patentable, as they have been separately argued as to patentability and they do not stand or fall together. In re Kaslow: 707 F2d 1366,1376, 201 ; USPQ 67, 70 (CCPA 1979), In re Dillon: 16 USPQ2nd 1897, 1900, CA FC 1990.

Since the elements in claim 1 comprise a combination which is functionally different from the suggested combination of Yausi US Patent 6594788 and the other references, for the reasons set forth above with respect to each of the claims, applicants respectfully submit that the combination defined by claim 1, and 2, 3,4,5,6 and 7 are also functionally different from the combination of Yausi US Patent 6594788 and the other references. Each claim solves or amplifies a solution to a different problem. Therefore, the 35 USC 103 rejection of each of the claims is requested to be requested to be withdrawn.

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The applicants feel that the Board of Appeals must conclude that the entire rejection fails.

(9) Appendix of Claims:

CLAIMS

Claim 1. (Currently Amended) A method for real time capture of the desired failing chip cell diagnostic information from high speed testing of a semiconductor chip, comprising the steps of:

collecting data from scanning the circuits of said semiconductor chip having LSSD diagnostic registers on chip for a failing cell for desired handling of multiple failures on a failing chip for immediate scan-out off-chip at a level of assembly test after scan initialization of the LSSD diagnostic registers on the semiconductor chip, said level of assembly test being selected from any level of a group consisting of: an initial manufacturing wafer test, a module test, a system level test, regardless of the clocking methodology, and

for the desired failing chip handling on chip of multiple bit failure detection:

providing data collection of a first failing cell in said LSSD diagnostic registers, and then skipping the collection of data up to a programmed amount to skip up to a subsequent failing cell, and

recording the failure of a next failing cell recognized after said subsequent failing cell in said LSSD diagnostic registers while making reuse of logic including existing address registers for providing data synchronous with fail determination circuits for data collection used for collection of data of said first failing cell, and then

pinpointing an actual failure for said next failing cell using additional data collected by reuse of the logic for data collection used for collection of data of said first failing cell

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2. (Previously Amended) The method according to claim 1 wherein the semiconductor chip is provided on chip with supplemental address registers which supplement said existing address registers for providing data synchronous with fail determination circuits, employing ABIST comparison circuit to obtain a bit wise fail result vector corresponding to each device data out of a device under test, and wherein said bit wise fail result vector feeds a detect and encode circuit that determines if one and only one device data out failed, and if so, provides an encoded "address" that is concatenated to a corresponding register address field.

3. (Previously Amended) The method according to claim 2 wherein said bit wise fail result vector is fed thereafter into a hold and compare function circuit having a hold portion of the function providing for the "full" fail address field comprising multiple bits of the memory address of the device under test plus the failing output encoded address for identifying the failing location to be stored in a LSSD register of said semiconductor chip, and wherein the compare function provides for identification recording of subsequent unique and different failing locations to be identified in the device under test.

4. (Previously Amended) The method according to claim 3 wherein said hold and compare function circuit is configured to load the first and reload each subsequent unique failing location encountered, decrementing a programmable skip counter at each unique fail encountered, until said programmable skip counter reaches a final "zero" state.

5. (Previously Amended) The method according to claim 4 wherein said hold and compare function circuit is configured to load the

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first and reload each subsequent unique failing location encountered, decrementing a programmable skip counter at each unique fail encountered, until the skip counter reaches an intended next failing cell recognized fail to be recorded.

6. (Original) The method according to claim 5 wherein said hold and compare function circuit allows said programmable skip counter to record a zero state as a default thus enabling the first fail to be recorded.

7. (Previously Amended) The method according to claim 2 wherein said supplemental address registers which supplement said existing address registers for providing data synchronous with fail determination circuits include a fail trap register, and there is provided a programmable skip counter, and a hold and compare function circuit, and wherein said programmable skip counter is enabled for initialization to a "record first fail" mode, and then with non-zero values of the programmable skip counter to a "record a next fail" mode, wherein said "record first fail" mode is considered the default or base function when the initial state of all registers is defined to be "0", and is obtained through scan initialization of the LSSD registers of the semiconductor chip

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(10) Items Not Affecting Merits- The typo correction of the dependency of claim 7 upon claim 7 is corrected in the appendix of claims. No other changes appear to be required.

(11) Table of Authorities:

35 USC 103

*Wright, in re:* 6 USPQ2d 1959, 1961, CA FC 1988.

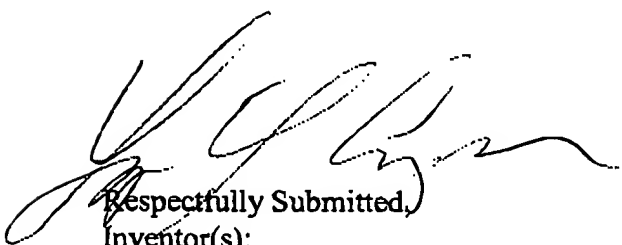
MPEP 706.02

*Ryco In. v. Av-Bar Corp.* 705 8 USPQ2d 1325

*In re Bond* 15 USPQ2d 1566, 1568 (FCCA 1990).

*In re Kaslow:* 707 F2d 1366, 1376, 201 USPQ 67, 70 (CCPA 1979)

*In re Dillon:* 16 USPQ2nd 1897, 1900, CA FC 1990.



Respectfully Submitted,

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